UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/071,860	02/08/2002	Thomas Bolt	Q02-1033-US1	1415

7590 01/13/2005

ROBERT A. SALTZBERG
MORRISON & FOERSTER LLP
425 MARKET STREET
SAN FRANCISCO, CA 94105

EXAMINER	
BUTLER, DENNIS	
ART UNIT	**PAPER NUMBER**
2115	

DATE MAILED: 01/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/071,860	Applicant(s) BOLT, THOMAS	
	Examiner Dennis M. Butler	Art Unit 2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 February 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. This action is in response to the application filed on February 8, 2002. Claims 1-32 are pending.

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 4, 6-8, 17, 19, 21-25, 27, 29-32 are rejected under 35 U.S.C. 102(e) as being anticipated by Stryker et al., U. S. Patent 6,460,099.

Per claim 1:

A) Stryker et al teach the following claimed items:

1. connecting three or more devices to an IDE bus (channel) with figures 1, 2A and 2B, at column 3, lines 7-35 and at column 4, lines 8-10;

2. configuring each device as Cable Select at column 4, lines 28-48;

3. a device controller that selectively activates at most two of the devices at the same time for data communication over the IDE bus with the controlling logic

of figures 2A and 2B, at column 4, lines 28-48 and at column 5, line 49 – column 6, line 24.

Per claims 4 and 6-8:

Stryker describes deactivating the remaining devices at column 4, lines 40-45. Stryker describes selecting each device via a selection signal (CSEL) comprising the cable select line at column 4, lines 28-48. Stryker describes that at least one of the devices is a disk drive with disk drive 30 of figure 1 and at column 3, lines 7-14.

Per claims 17 and 25:

A) Stryker et al teach the following claimed items:

1. an IDE interface system (ATA system) having three or more devices (ATA mass storage devices) connected to an IDE bus (ATA channel) with figures 1 and 2A, at column 3, lines 7-35 and at column 4, lines 8-10;

2. a device controller for receiving device control signals to select at least one of the devices for data communication with the processor (Host Processor System 50) with the controlling (decoding, detecting and isolation) logic of figure 2A, with figures 5A and 5B, at column 4, lines 28-48 and at column 5, line 49 – column 6, line 24;

3. the device controller selectively activating at most two of the devices at the same time for data communication with the controlling logic of figure 2A, with figures 5A and 5B, at column 4, lines 28-48 and at column 5, lines 49–57.

Per claims 19, 21-24, 27 and 29-32:

Stryker describes deactivating the remaining devices at column 4, lines 40-45. Stryker describes selecting each device via a selection signal (CSEL) comprising the cable select line at column 4, lines 28-48. Stryker describes an interface controller connected to the devices via the IDE bus (ATA channel) that manages information flow between the processor and the devices over the IDE bus with figures 2A, 5A and 5B, at column 4, lines 8-27 and at column 7, lines 17-43. Stryker describes that at least one of the devices is a disk drive with disk drive 30 of figure 1 and at column 3, lines 7-14.

5. Claims 2-3, 5, 18, 20, 26 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stryker et al., U. S. Patent 6,460,099 in view of Chong, Jr., U. S. Patent 6,697,867.

Per claims 2-3, 18 and 26:

The claims seem to differ from Stryker in that Stryker fails to explicitly teach identifying and selecting devices as master and slave devices and activating the selected devices for communication with the processor as claimed. However, Chong, Jr. describes receiving device control signals to select one or two of the devices for data communication with the processor (CPU 12) with ATA Host Adapter 16 of figure 1 and at column 6, lines 1-11, selecting one of the devices as a master device and the second device as a slave device and activating at most two of the devices at the same time for data communication with the processor at column 6, lines 12-65. Chong, Jr. describes deactivating (deasserting) non-selected devices at column 6, lines 44-53. Chong, Jr.

describes a selection signal for each of the two devices with the CS signals that correspond to each of the devices at column 6, lines 12-65. It would have been obvious to one having ordinary skill in the art at the time the invention was made to identify and select devices as master and slave devices and activate the selected devices for communication with the processor, as taught by Chong, Jr., in order to allow access to both a master drive and a slave drive and increase the amount of storage allowed to be accessed at the same time. One of ordinary skill in the art would have been motivated to combine Stryker and Chong, Jr. because of Chong, Jr.'s suggestion of providing plural master/slave groups at column 1, lines 26-28 and at column 2, lines 7-46. It would have been obvious for one of ordinary skill in the art to combine Chong, Jr. and Stryker because they are both directed to the problem of increasing the ATA/IDE connection capabilities by allowing more than two devices to be connected and accessible over a single ATA interface and ATA bus.

Per claims 5, 20 and 28:

The claims seem to differ from Stryker in that Stryker fails to explicitly teach activating the selected devices by powering the devices on and deactivating the remaining devices by powering them off as claimed. Stryker describes four methods of activating and deactivating ATA devices including using the CSEL line, intercepting the DRV/HD command and using Q-switches. Chong, Jr. describes activating and deactivating ATA devices using group access signals, a control register, routing logic and chip select signals. Neither Stryker nor Chong,

Jr. describe activating/deactivating the devices by powering the devices on/off. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to activate the selected devices by powering the devices on and deactivate the remaining devices by powering them off because it is well known and inherent that ATA devices cannot be active when they are powered off and using the device power inputs for activating and deactivating the devices would reduce the power consumption of the ATA/IDE system.

6. Claims 17-19, 21, 23-27, 29 and 31-32 are rejected under 35 U.S.C. 102(e) as being anticipated by Chong, Jr., U. S. Patent 6,697,867.

Per claims 17 and 25:

A) Chong, Jr. teaches the following claimed items:

1. an IDE interface system (ATA system) having three or more devices (ATA Devices 20A-D) connected to an IDE bus (ATA channel) with figure 1, at column 1, lines 13-25 and at column 5, lines 13-44;

2. a device controller for receiving device control signals to select at least one of the devices for data communication with the processor (CPU 12) with ATA Host Adapter 16 of figure 1 and at column 6, lines 1-11;

3. the device controller selectively activating at most two of the devices at the same time for data communication with the processor at column 6, lines 12-65.

Per claims 18-19, 21, 23-24, 26-27, 29 and 31-32:

Chong, Jr. describes receiving device control signals to select one or two of the devices for data communication with the processor (CPU 12) with ATA Host

Adapter 16 of figure 1 and at column 6, lines 1-11, selecting one of the devices as a master device and the second device as a slave device and activating at most two of the devices at the same time for data communication with the processor at column 6, lines 12-65. Chong, Jr. describes deactivating (deasserting) non-selected devices at column 6, lines 44-53. Chong, Jr. describes a selection signal for each of the two devices with the CS signals that correspond to each of the devices at column 6, lines 12-65. Chong, Jr. describes an interface controller connected to devices via the IDE bus for managing information flow between the processor and the devices with figure 1, at column 1, lines 13-25 and at column 5, lines 13-44. Chong, Jr. describes that at least one device is a disk drive at column 5, lines 59-67.

7. Claims 9-12 and 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chong, Jr., U. S. Patent 6,697,867 in view of Chu et al., U.S. Patent 6,725,385.

Per claims 9-11:

A) Chong, Jr. teaches the following claimed items:

1. an IDE system (ATA system) having three or more devices (ATA Devices 20A-D) connected to an IDE bus (ATA channel) with figure 1, at column 1, lines 13-25 and at column 5, lines 13-44;

2. identifying devices, selecting one of the devices as a master device and a second device as a slave device at column 6, lines 1-65,

3. activating at most two of the selected devices at the same time for data communication with the processor at column 6, lines 12-65.

B) The claim seems to differ from Chong, Jr. in that Chong, Jr. fails to explicitly describe deactivating all of the devices as claimed.

C) However, Chong, Jr. describes activating a device group using a group access signal and deactivating the remaining groups with corresponding group access signals at column 2, lines 25-34. Therefore, Chong, Jr. discloses the claimed invention except for explicitly reciting that all of the devices are deactivated. Chu et al teach that it is known to deactivate all ATA devices connected to an ATA/IDE bus with figures 1 through 3, at column 1, lines 13-53, at column 2, lines 12-30 and at column 3, lines 45-67. In addition, Chu describes that deactivating all devices is a design choice based on a trade-off between energy consumption and response time of the devices at column 1, lines 13-19. It would have been obvious to one having ordinary skill in the art at the time the invention was made to deactivate all of the devices, as taught by Chu, in order to reduce the energy consumption of the devices connected to the IDE/ATA bus. One of ordinary skill in the art would have been motivated to combine Chong, Jr. and Chu because of Chu's suggestion that deactivating all devices connected to an ATA/IDE bus would reduce energy consumption of the system at column 1, lines 36-53 and at column 2, lines 54-65. It would have been obvious for one of ordinary skill in the art to combine Chong, Jr. and Chu because they are both directed to the problem of activating and deactivating ATA/IDE devices

connected to an ATA bus. Furthermore, Chong, Jr. describes activating a device group based on a corresponding group access signal received from the host over the ATA interface at column 2, lines 15-18 and 25-34 and Chu describes providing monitoring logic that activates a device based on a predetermined communication signal over the ATA interface at column 2, lines 23-30. Therefore, the ATA power control features of Chu can be readily incorporated into the ATA interface of Chong, Jr.

Per claims 12 and 16:

Chong, Jr. describes connecting three or more devices to the IDE bus (ATA channel) at column 5, lines 36-44. Chong, Jr. describes that at least one device is a disk drive at column 5, lines 59-67.

Per claim 15:

Chu describes deactivating each device by powering them off and activating each selected device by powering them on with figure 2 and at column 6, lines 21-65.

8. Claims 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chong, Jr., U. S. Patent 6,697,867 in view of Chu et al., U.S. Patent 6,725,385 and further in view of Stryker et al., U. S. Patent 6,460,099.

Per claims 13 and 14:

The claim seems to differ from Chong, Jr. in view of Chu in that Chong, Jr. in view of Chu fails to explicitly describe configuring each device as cable select, selecting the first device as a master via the cable select signal and selecting the

second device as slave via the cable select signal as claimed. Stryker teaches configuring each device as Cable Select at column 4, lines 28-48. Stryker describes configuring/selecting each device as a master (device 0) or a slave (device 1) with figures 5A and 5B, at column 3, lines 25-28, at column 4, lines 28-48 and at column 7, lines 17-43. It would have been obvious to one having ordinary skill in the art at the time the invention was made to configure each device as cable select, select the first device as a master via the cable select signal and select the second device as slave via the cable select signal, as taught by Stryker, in order to dynamically select a first device as the master device and a second device as a slave device. One of ordinary skill in the art would have been motivated to combine Stryker and Chong, Jr. because of Chong, Jr.'s suggestion of providing plural master/slave groups at column 1, lines 26-28 and at column 2, lines 7-46. It would have been obvious for one of ordinary skill in the art to combine Chong, Jr. and Stryker because they are both directed to the problem of increasing the ATA/IDE connection capabilities by allowing more than two devices to be connected and accessible over a single ATA interface and ATA bus.

9. Claims 20, 22, 28 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chong, Jr., U. S. Patent 6,697,867 in view of Stryker et al., U. S. Patent 6,460,099.

Per claims 20 and 28:

The claims seem to differ from Chong, Jr. in that Chong, Jr. fails to explicitly teach activating the selected devices by powering the devices on and deactivating the remaining devices by powering them off as claimed. Stryker describes four methods of activating and deactivating ATA devices including using the CSEL line, intercepting the DRV/HD command and using Q-switches. Chong, Jr. describes activating and deactivating ATA devices using group access signals, a control register, routing logic and chip select signals. Neither Stryker nor Chong, Jr. describe activating/deactivating the devices by powering the devices on/off. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to activate the selected devices by powering the devices on and deactivate the remaining devices by powering them off because it is well known and inherent that ATA devices cannot be active when they are powered off and using the device power inputs for activating and deactivating the devices would reduce the power consumption of the ATA/IDE system. One of ordinary skill in the art would have been motivated to combine Stryker and Chong, Jr. because of Chong, Jr.'s suggestion of providing plural master/slave groups at column 1, lines 26-28 and at column 2, lines 7-46. It would have been obvious for one of ordinary skill in the art to combine Chong, Jr. and Stryker because they are both directed to the problem of increasing the ATA/IDE connection capabilities by allowing more than two devices to be connected and accessible over a single ATA interface and ATA bus.

Per claims 22 and 30:

Stryker describes selecting each device via a selection signal (CSEL) comprising the cable select line at column 4, lines 28-48.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dennis M. Butler whose telephone number is 571-272-3663. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Dennis M. Butler
Dennis M. Butler
Primary Examiner
Art Unit 2115